MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}			

FUNCTION DESCRIPTION

The HCT161A/163A are programmable 4–bit synchronous counters that feature parallel Load, synchronous or asynchronous Reset, a Carry Output for cascading and count–enable controls.

The HCT161A and HCT163A are binary counters with asynchronous Reset and synchronous Reset, respectively.

INPUTS

Clock (Pin 2)

The internal flip–flops toggle and the output count advances with the rising edge of the Clock input. In addition, control functions, such as resetting and loading occur with the rising edge of the Clock input. In addition, control functions, such as resetting (HCT163A) and loading occur with the rising edge of the Clock Input.

Preset Data Inputs P0, P1, P2, P3 (Pins 3, 4, 5, 6)

These are the data inputs for programmable counting. Data on these pins may be synchronously loaded into the internal flip–flops and appear at the counter outputs. P0 (Pin 3) is the least–significant bit and P3 (Pin 6) is the most–significant bit.

OUTPUTS

Q0, Q1, Q2, Q3 (Pins 14, 13, 12, 11)

These are the counter outputs. Q0 (Pin 14) is the least–significant bit and Q3 (Pin 11) is the most–significant bit.

Ripple Carry Out (Pin 15)

When the counter is in its maximum state 1111, this output goes high, providing an external look–ahead carry pulse that may be used to enable successive cascaded counters. Ripple Carry Out remains high only during the maximum count state. The logic equation for this output is:

Ripple Carry Out = Enable T ωQ0 ωQ1 ωQ2 ωQ3

CONTROL FUNCTIONS

Resetting

A low level on the Reset pin (pin 1) resets the internal flip–flops and sets the outputs (Q0 through Q3) to a low level. The HCT161A resets asynchronously, and the HCT163A resets with the rising edge of the Clock input (synchronous reset).

Loading

With the rising edge of the Clock, a low level on Load (pin 9) loads the data from the Preset Data input pins (P0, P1, P2, P3) into the internal flip–flops and onto the output pins, Q0 through Q3. The count function is disabled as long as Load is low.

Count Enable/Disable

These devices have two count–enable control pins: Enable P (Pin 7) and Enable T (Pin 10). The devices count when these two pins and the Load pin are high. The logic equation is:

Count Enable = Enable P ωEnable T ωLoad

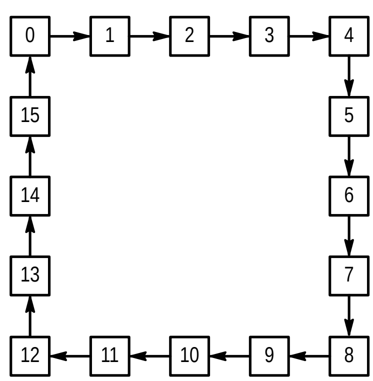
The count is either enabled or disabled by the control inputs according to Table 1. In general, Enable P is a count–enable control: Enable T is both a count–enable and a Ripple–Carry Output control.

Table 1. Count Enable/Disable

Control Inputs			Result at Outputs	
Load	Enable P	Enable T	Q0–Q3	Ripple Carry Out
H	H	H	Count	High when Q0–Q3 are maximum*
L	H	H	No Count	
X	L	H	No Count	High when Q0–Q3 are maximum*
X	X	L	No Count	L

Q0 through Q3 are maximum when Q3 Q2 Q1 Q0 = 1111.

OUTPUT STATE DIAGRAM



Binary Counters

SWITCHING WAVEFORMS

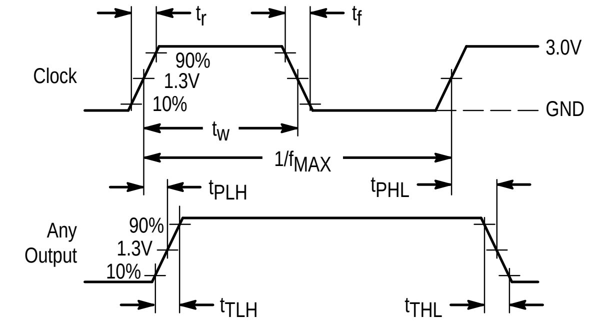


Figure 1.

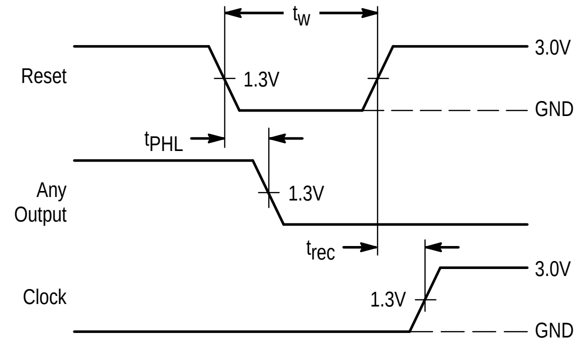


Figure 2.

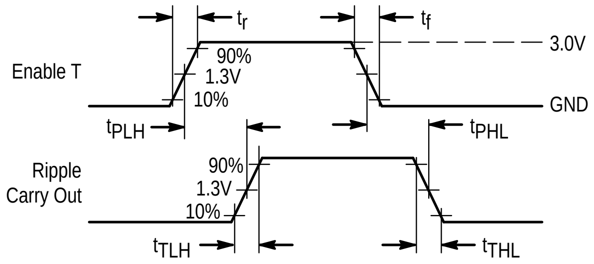


Figure 3.

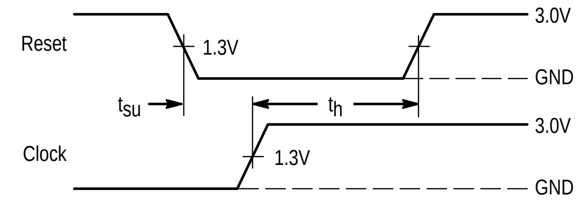


Figure 4. HCT163A Only

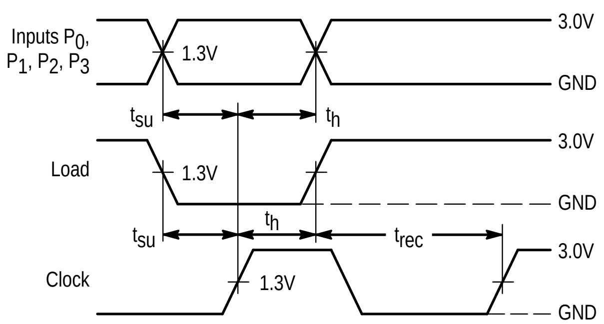


Figure 5.

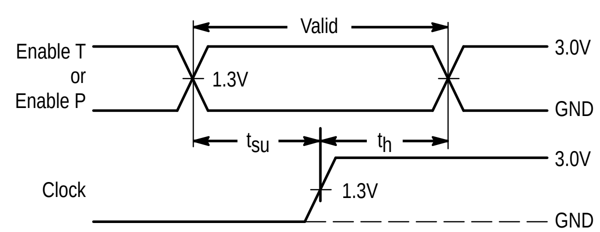
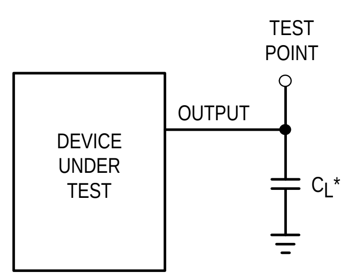
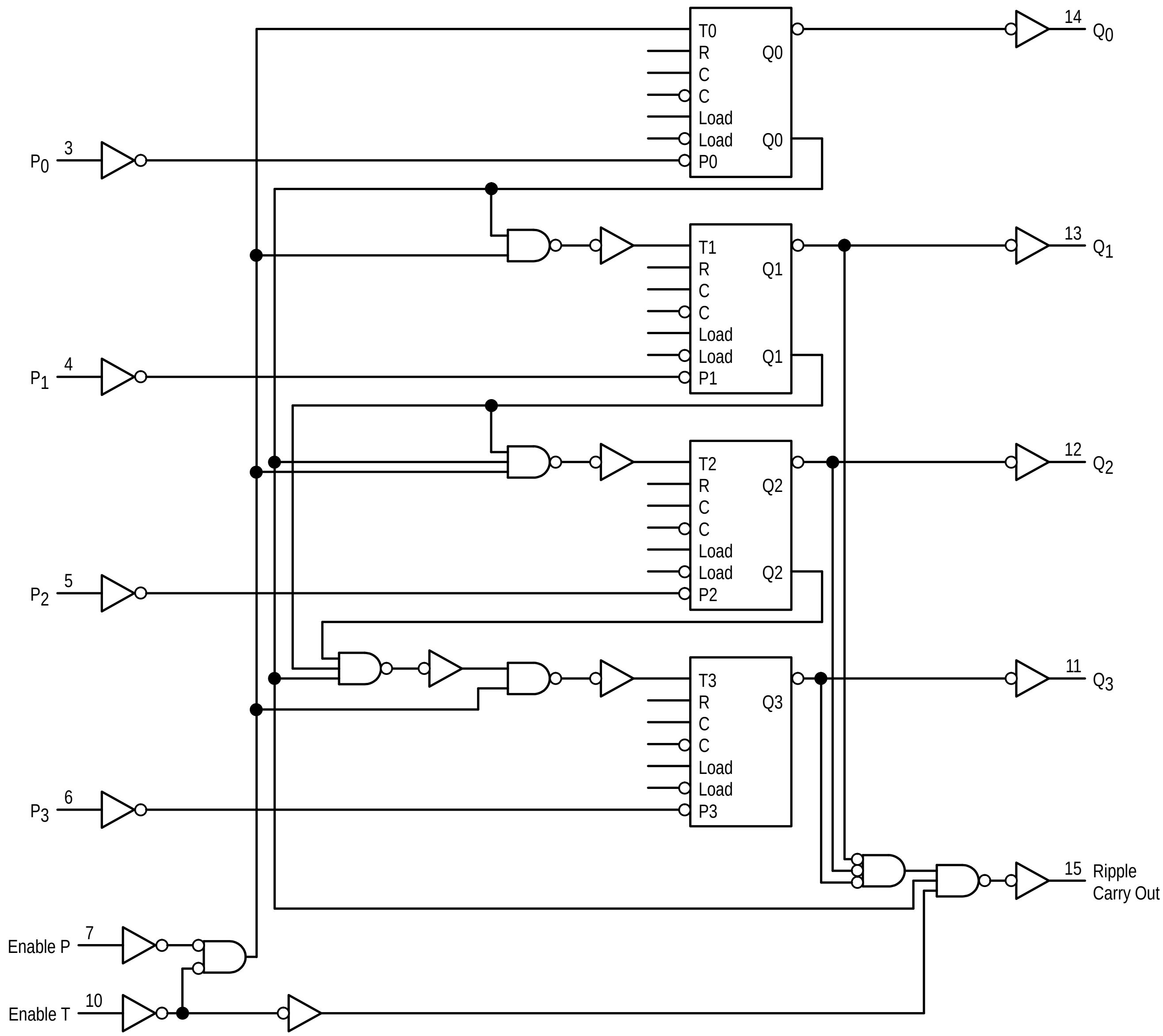


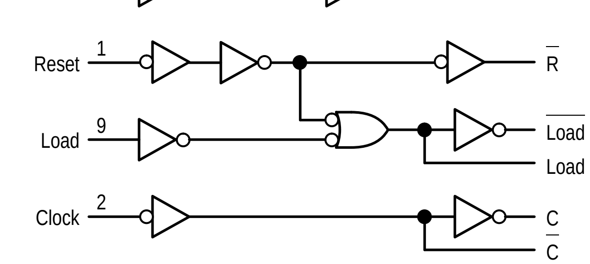
Figure 6.



*Includes all probe and jig capacitance

Figure 7. Test Circuit





The flip–flops shown in the circuit diagrams are Toggle–Enable flip–flops. A Toggle–Enable flip–flop is a combination of a D flip–flop and a T flip–flop. When loading data from Preset inputs P_0, P_1, P_2 and P_3, the Load signal is used to disable the Toggle input (T_n) of the flip–flop. The logic level at the P_n input is then clocked to the Q output of the flip–flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip–flop low.

Figure 8. 4–Bit Binary Counter with Asynchronous Reset (MC54/74HCT161A)

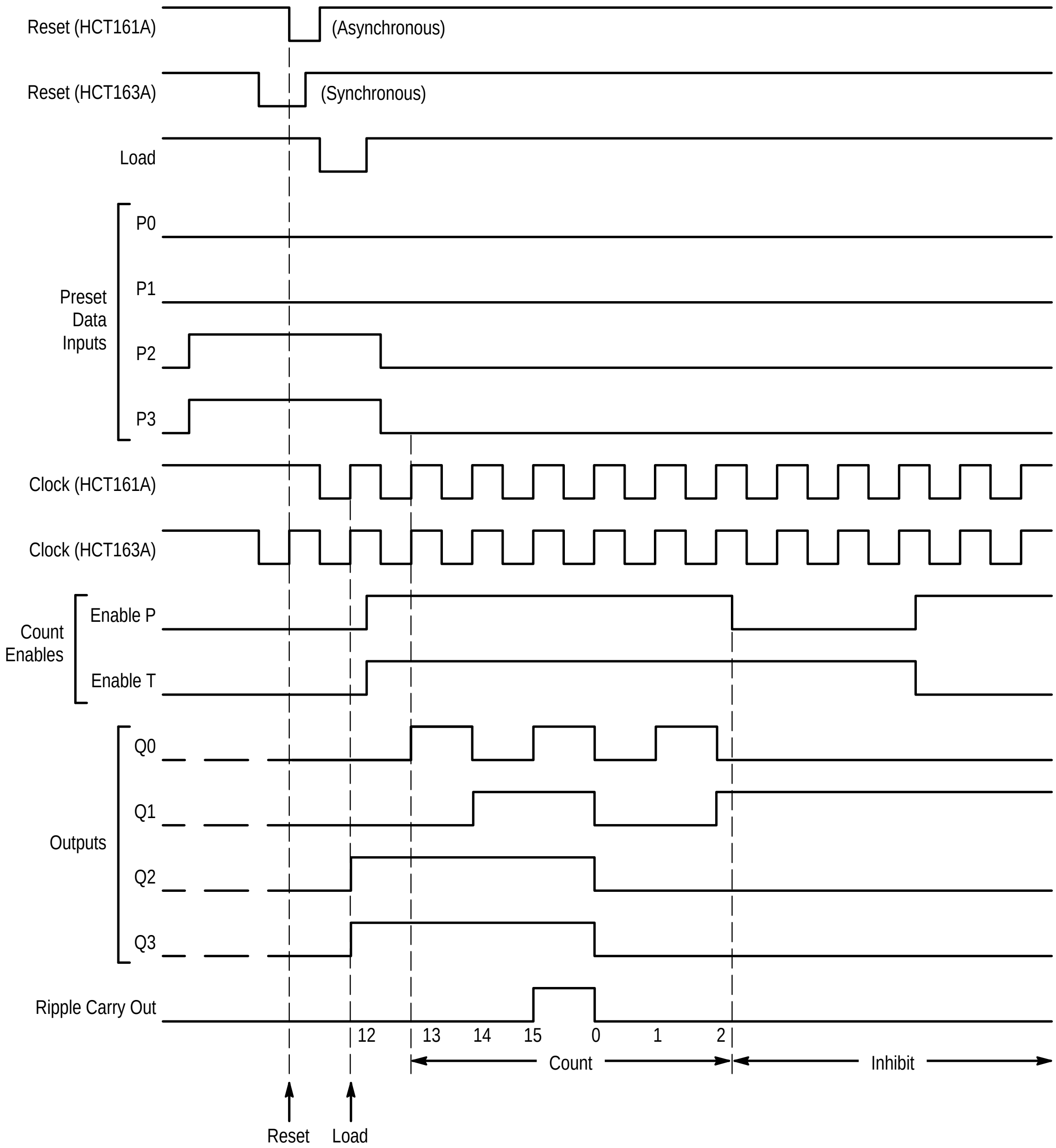
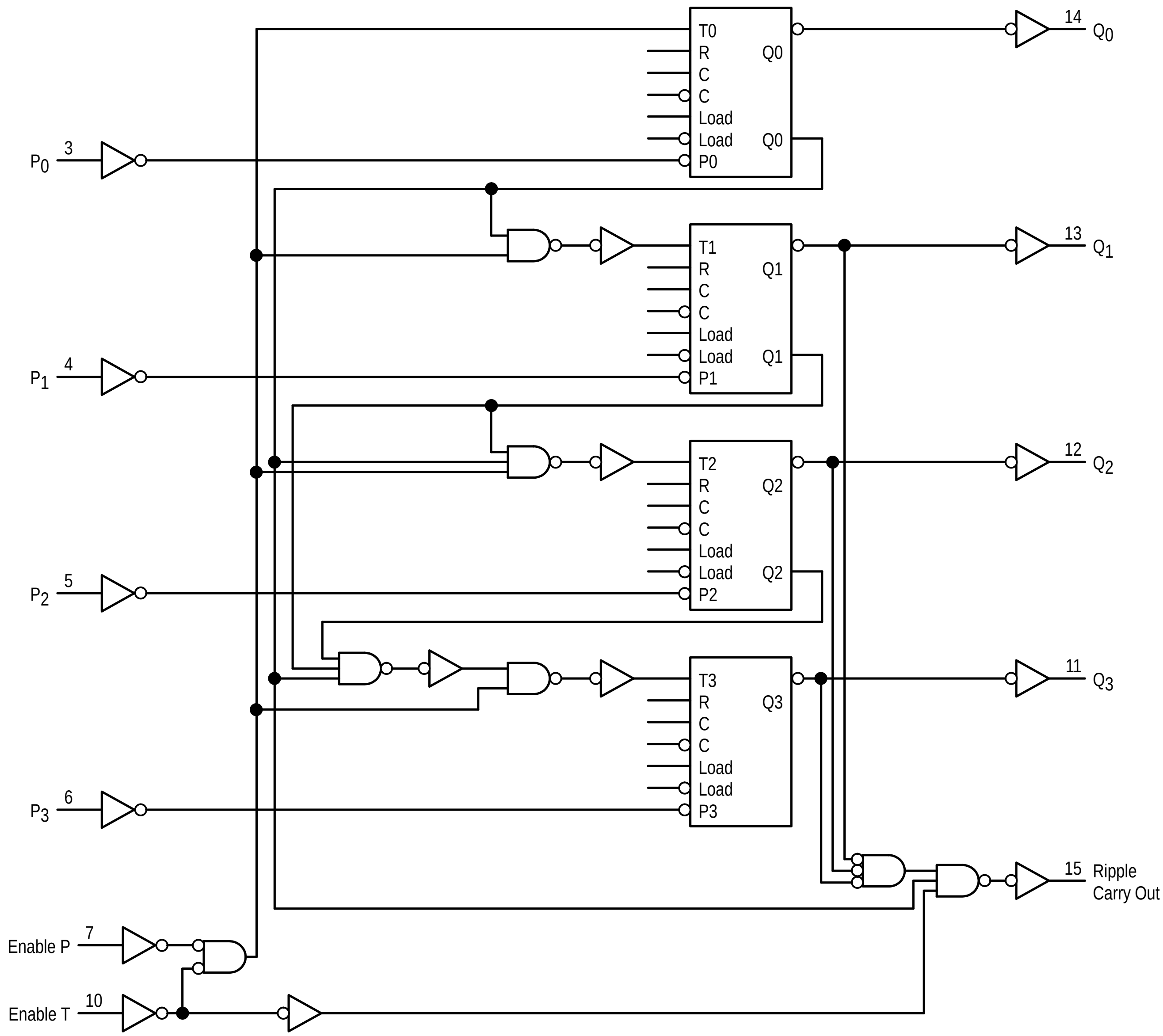
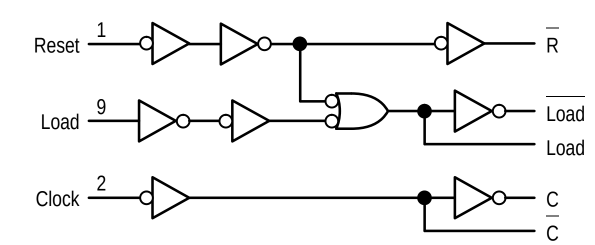


Figure 9. Timing Diagram



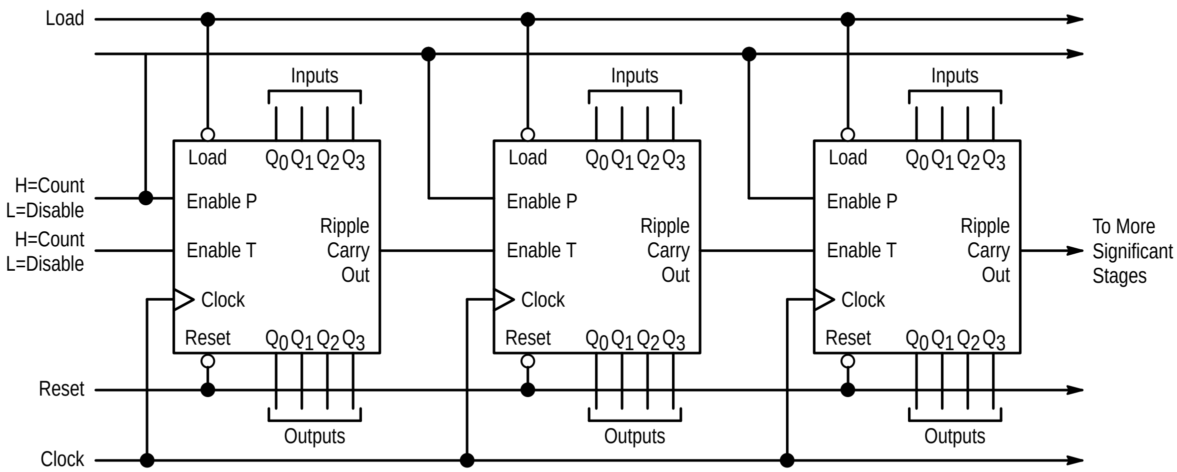


The flip–flops shown in the circuit diagrams are Toggle–Enable flip–flops. A Toggle–Enable flip–flop is a combination of a D flip–flop and a T flip–flop. When loading data from Preset inputs P_0, P_1, P_2 and P_3, the Load signal is used to disable the Toggle input (T_n) of the flip–flop. The logic level at the P_n input is then clocked to the Q output of the flip–flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip–flop low.

Figure 10. 4–Bit Binary Counter with Synchronous Reset (MC54/74HCT163A)

TYPICAL APPLICATIONS CASCADING



NOTE: When used in these cascaded configurations the clock f_{max} guaranteed limits may not apply. Actual performance will depend on number of stages. This limitation is due to set–up times between Enable (port) and clock.

Figure 11. N–Bit Synchronous Counters

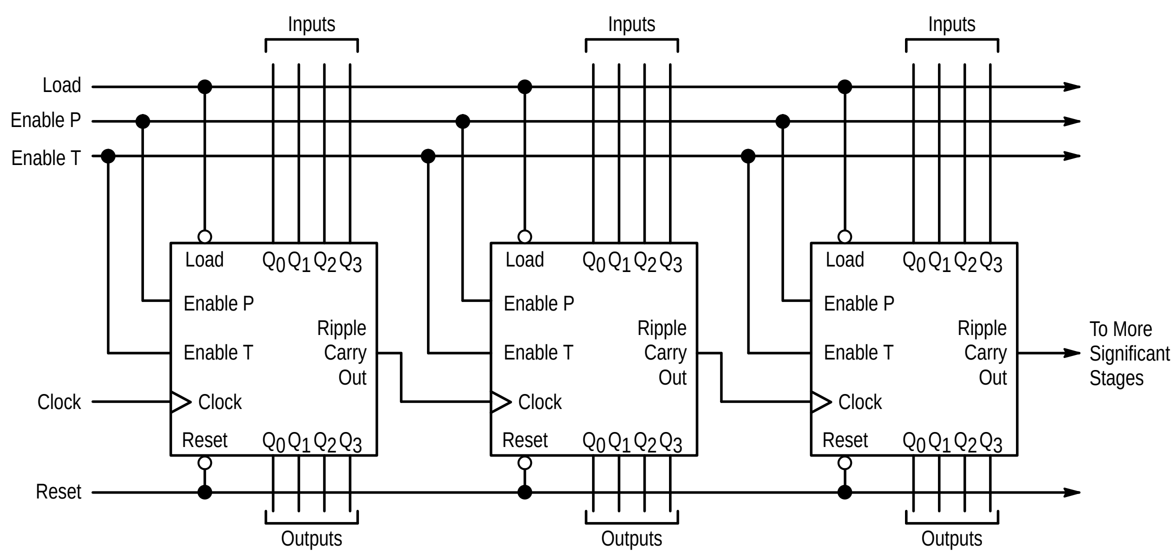


Figure 12. Nibble Ripple Counter

TYPICAL APPLICATIONS VARYING THE MODULUS

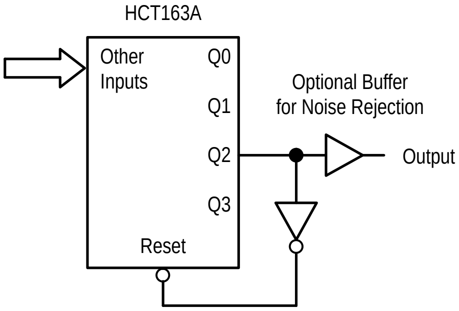


Figure 13. Modulo–5 Counter

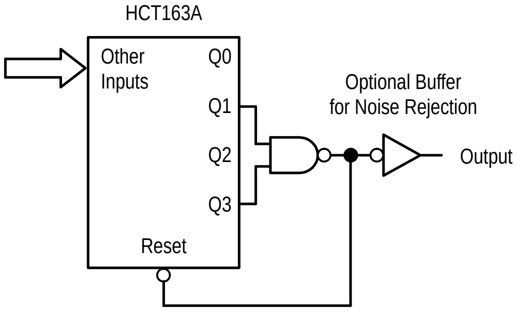
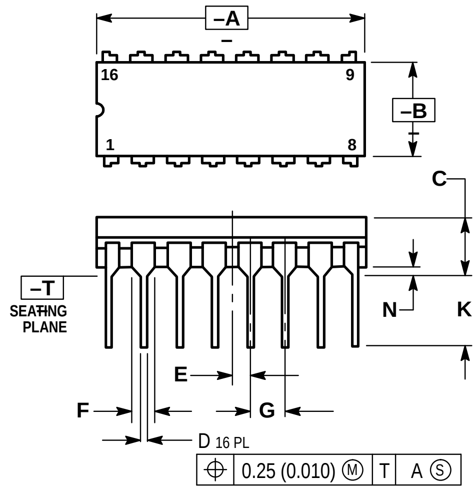


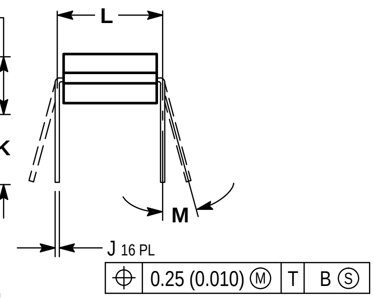
Figure 14. Modulo–11 Counter

The HCT163A facilitates designing counters of any modulus with minimal external logic. The output is glitch–free due to the synchronous Reset.

OUTLINE DIMENSIONS

J SUFFIX
CERAMIC PACKAGE
CASE 620–10
ISSUE V

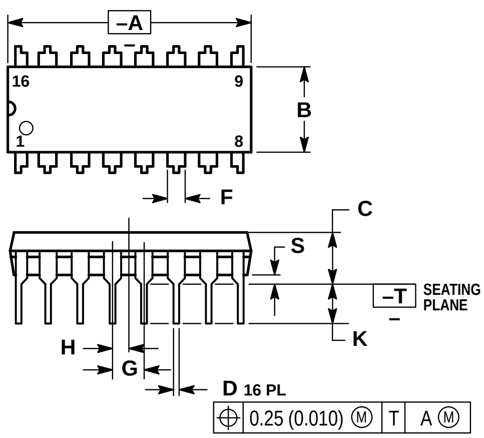


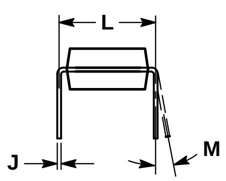


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	05	155	05	155
N	0.020	0.040	0.51	1.01

N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R

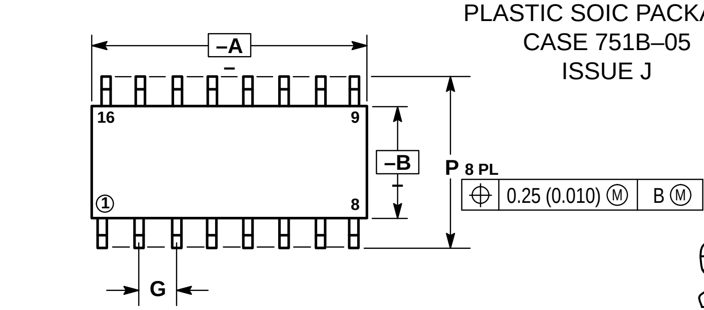


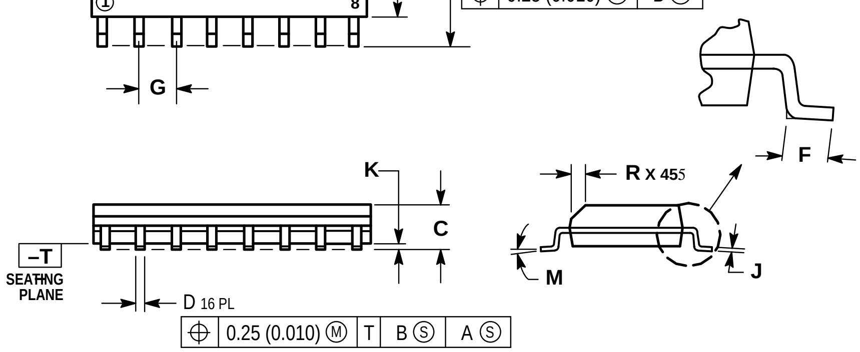


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	05	105	05	105
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	05	75	05	75
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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